UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,439	09/29/2005	Shinobu Kato	278942US90PCT	3042

22850 7590 02/20/2009

OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
02/20/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/551,439	KATO, SHINOBU	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-17* is/are pending in the application.

4a) Of the above claim(s) *7 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,9 and 11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to amendment filed on November 13, 2008.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 16 and 17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 16, the structure recited by “wherein the core substrate is so constructed that the conductive layer of the inner layer is formed on each of both sides of a metallic plate electrically insulating, through resin layer and further, the conductive layer on the surface side is formed outside the conductive layer of the inner layer through resin layer” is unclear. As the base claim 12 recites core made of multiple layers. The structure of additional core plate is unclear.

Regarding claim 17, the structure recited by " the core substrate is so constructed that a thick conductive layer is disposed as the inner layer and a thin conductive layer is disposed on the surface side" is unclear. The base claim 12 recites core substrate composed of three or more layers including a thick conductive layer as an inner layer. It is unclear if a thick conductive layer is disposed as the inner layer and

a thin conductive layer are different layers and if so, how they are related to those recited in claim 12.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 4, 5, 6 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe (US Patent No. 6,333,857).

Regarding claim 1, Kanbe in figure 2 discloses a multi-layer printed wiring board comprising: a core substrate (110) having a plurality of through holes (107) therein the through holes in the core substrate being disposed so that a ground through hole and a power through hole adjoin each other (see figure 10);

an interlayer insulating layer (121, figure 8) formed on the core substrate; a conductive layer (101, 106) formed on the interlayer insulating layer; and a plurality of via holes provided in the insulating layer and configured to provide electrical connection between the conductive layer and through holes (see figure).

Kanbe does not disclose a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm. However, the distance will be decided

based on the space available in the board to avoid shorting of the adjacent pad on via during operation as well as better routing of the traces.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Kanbe with a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm in order to avoid short circuit of the adjacent pad on via during operation to accommodate the via holes in the available space in the board.

Regarding claim 2, the modified board of Kanbe further discloses the ground through hole in the core substrate including two or more ground through holes and the power through hole including two or more power through holes (see figure 2), such that the ground through holes and the power through holes are disposed in a grid formation or in a staggered formation at adjacent positions (see figure 10).

Regarding claim 4, the modified board of Kanbe further discloses the diameter of the ground through hole is 50 to 500 μm and the diameter of the power through hole is 50 to 500 μm ((column 19, line 5-10).

Regarding claim 5, the modified board of Kanbe further discloses at least one through of the ground through holes and the power through holes comprises, two or more through holes in a stack structure through all layers of the multi-layer printed wring board up to outermost layer (see figure 8).

Regarding claim 6, the modified board of Kanbe discloses all the features of the claimed invention including the ground through hole and the power through hole, but does not explicitly disclose any IC chip mounted on the board. However, it is old and known in the art to mount chip on the upper surface of a board for necessary interconnection. Mounting a chip on the board will meet the requirement of the via holes below the chip.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to have the modified board of Kanbe with an IC chip on the board, which meets the limitation that the ground through hole and the power through hole will be below chip, in order to have necessary interconnection.

Regarding claim 11, the modified board of Kanbe discloses all the features of the claimed invention but does not disclose a capacitor mounted on the surface thereof. However, mounting capacitors on the board is old and known in art to control the noise.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board Kanbe with a capacitor mounted on the surface thereof, in order to control the noise.

Regarding claim 12, the modified board of Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three or more layers and including a thick conductive layer as an inner layer, and the conductive layer of each

inner layer of the core substrate and the conductive layer of each surface are conductive layer for power layer or conductive layer for grounding (see figure 1 and 2).

Regarding claim 13, the modified board of Kanbe further discloses the core substrate (110) is a multi-layer core substrate composed of three layers and including a thick conductive layer as an inner layer, and the conductive layer of each inner layer of the core substrate is conductive layer for power layer or conductive layer for grounding (see figure 1 and 2) and the conductive layer on the front surface side is composed of signal line (via 107 is connected to signal line, figure 1).

6. Claims 8, 9 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe as applied to claims 1 and 12 above, and further in view of Strandberg (US Patent No. 6,323,435).

Regarding claims 8, 9 and 14, Kanbe discloses all the features of the claimed invention as applied to claim 1 but does not disclose the relationship between the conductive layer on the core substrate and on the insulating layer as recited in claims 8, 9 and 14.

However, as disclosed by Strandberg in figure 1, it is known in the art to have the conductive layer formed in the buildup portion thinner than that the layer formed in the core substrate to have high density interconnect.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the conductive layer formed on interlayer

insulating resin thinner than that of the layer in the core substrate, meeting the relationship as recited in claim 8, and 14, as taught by Strandberg, in order to have high density interconnect.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 223, 235 (CCCPA 1955).

Regarding claim 15, the modified board of Kanbe further discloses the conductive layer in the inner layer of the core substrate is composed on two or more layers as applied to claim 12 above.

Regarding claim 16, the modified board of Kanbe discloses all the features of the claimed invention as applied to claim 12 above but does not discloses a metallic plate in the core layer. However, providing a metallic plate in the core substrate is old and known in the art to have mechanical stability of the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the board of Kanbe with a metallic plate as recited in claim 16, in order to have better mechanical stability of board.

Regarding claim 17, the modified board of Kanbe discloses all the features of the claimed invention as applied to claim 12 above but does not discloses the core

substrate is so constructed that a thick conductive layer is disposed as the inner layer and a thin conductive layer is disposed on the surface side. However, providing a thick conductive layer as an inner layer will provide better mechanical stability.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified board of Kanbe with a thick conductive layer disposed as the inner layer and a thin conductive layer disposed on the surface side, in order to have better mechanical stability.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) / new explanation of rejection.

Further, applicant on page 8 of the response, argues that since Kanbe utilizes the laminated capacitor in the core substrate to solve the problem of noise or delay of power supply to the IC chip which causes switch errors. Therefore, there is not need in Kanbe to provide particular distance requirement between power and ground through holes.

This is not found to be persuasive.

There are various criteria for maintaining distance between the via holes. One of criteria is to keep a distance to avoid shorting of the adjacent pad on via during operation or during solder connection or to help better routing of the traces. Use of laminated capacitor does not exclude other criteria to be met.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Iijima (US Patent Application Publication No. 2003/0011070) in figure (1A) discloses a conventional board with distance between the via hole of 400 μm and in figure (3A) a board with the distance between the via hole of 100 μm.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ibp
February 16, 2009

/Ishwar (I. B.) Patel/
Primary Examiner, Art Unit 2841